EXHIBIT J

United States Patent [19]

Colak

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[54] **LATERAL DOUBLE-DIFFUSED MOS TRANSISTOR DEVICES SUITABLE FOR SOURCE-FOLLOWER APPLICATIONS**

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[73] Assignee: **North American Philips Corporation, New York, N.Y.**

[21] Appl. No.: **766,665**

[22] Filed: **Aug. 15, 1985**

Related U.S. Application Data

[63] Continuation of Ser. No. 451,993, Dec. 21, 1982, abandoned.

[51] Int. Cl.[4] H01L 29/94

[52] U.S. Cl. 357/23.4; 357/23.8; 357/23.14; 357/13

[58] Field of Search 357/23.4, 23.8

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,292,642	9/1981	Appels et al.	357/13
4,300,150	11/1981	Colak	357/13
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Pocha et al, "Tradeoff Between Threshold Voltage and Breakdown in High Voltage Double-Diffused MOS Transistors", *IEEE Trans. on Elec. Dev.*, vol. ED25, No. 11, Nov. 1978.

Colak et al., "Lateral DMOS Power Transistor Design", *IEEE Electron Device Letters*, vol. EDL-1, No. 4, Apr. 80.

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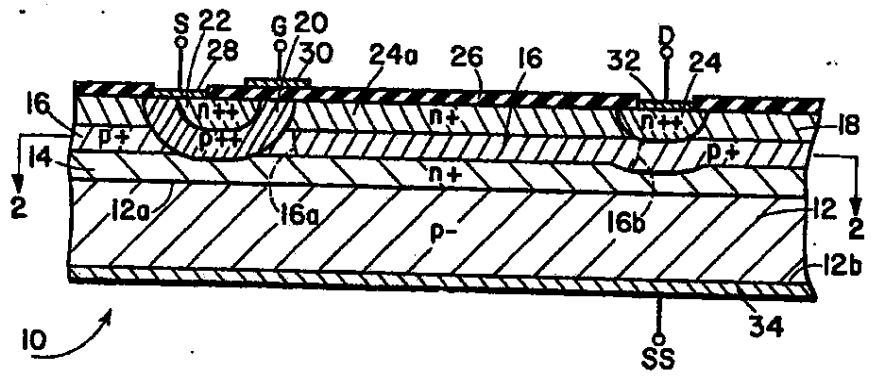
[57] **ABSTRACT**

A lateral double-diffused MOS transistor includes an intermediate semiconductor layer of the same conductivity type as the channel region which extends laterally from the channel region to beneath the drain contact region of the device. This intermediate semiconductor layer substantially improves the punchthrough and avalanche breakdown characteristics of the device, thus permitting operation in the source-follower mode, while also providing a compact structure which features a relatively low normalized "on" resistance.

12 Claims, 5 Drawing Figures



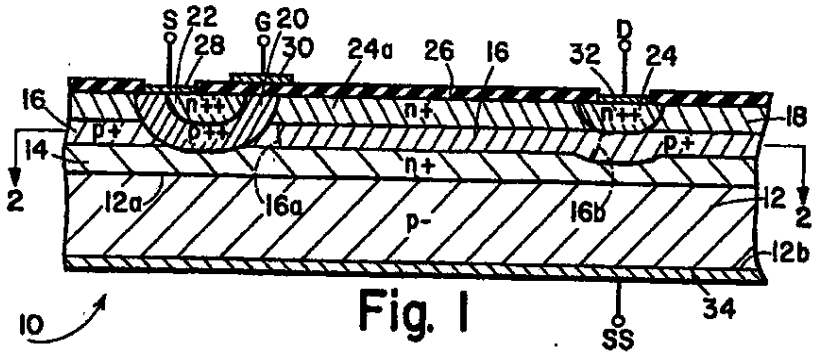


Fig. 1

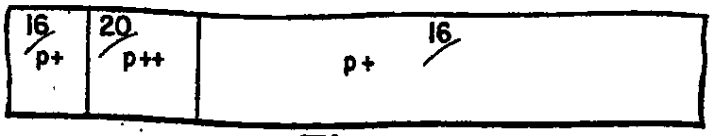


Fig. 2A

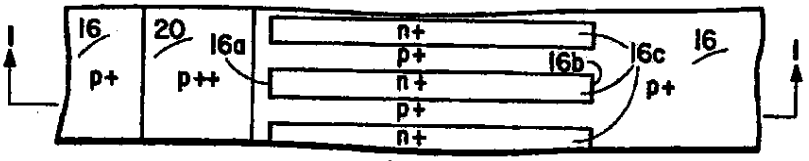


Fig. 2B

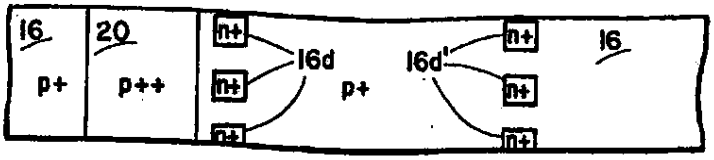


Fig. 2C

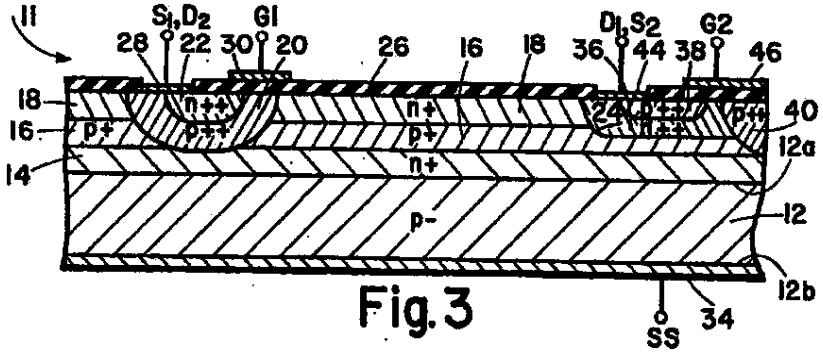


Fig. 3

LATERAL DOUBLE-DIFFUSED MOS TRANSISTOR DEVICES SUITABLE FOR SOURCE-FOLLOWER APPLICATIONS

This is a continuation of application Ser. No. 451,993, filed Dec. 21, 1982, now abandoned.

BACKGROUND OF THE INVENTION

The invention is in the field of metal-oxide-semiconductor (MOS) field-effect devices, and relates specifically to lateral double-diffused MOS (DMOS) field-effect transistors suitable for use in source-follower applications.

A typical prior-art high voltage DMOS transistor is shown on page 1325 of the "IEEE Transactions on Electron Devices", Vol. ED-25, No. 11, November 1978, in a paper entitled "Tradeoff Between Threshold Voltage and Breakdown in High-Voltage Double-Diffused MOS Transistors", by Pocha et al. This device includes a semiconductor substrate of a first conductivity type (p-type), a surface layer of a second conductivity type (n-type) on the substrate, a surface-adjoining channel region of the first conductivity type in the epitaxial layer, a surface-adjoining source region of the second conductivity type in the channel region, and a surface-adjoining drain contact region of the second conductivity type in the epitaxial layer and spaced apart from the channel region. An insulating layer is provided on the surface layer and covers at least that portion of the channel region located between the source and drain. A gate electrode is provided on the insulating layer, over a portion of the channel region between the source and drain and is electrically isolated from the surface layer, while source and drain electrodes are connected respectively to the source and drain regions of the transistor. Such prior-art high-voltage DMOS transistors have a relatively thick surface layer (typically an epitaxial layer), in the order of about 25–30 microns for a breakdown voltage of about 250 V, as indicated in the Pocha et al paper. Furthermore, the punchthrough and avalanche breakdown characteristics of these devices relative to their epitaxial layer thickness make them unsuitable for efficient use in applications requiring high voltages.

It has been found that the breakdown characteristics of high-voltage semiconductor devices can be improved using the REduced SURface Field (or RESURF) technique, as described in "High Voltage Thin Layer Devices (RESURF Devices)", "International Electronic Devices Meeting Technical Digest", December 1979, pages 238–240, by Appels et al, and U.S. Pat. No. 4,292,642 to Appels et al. Essentially, the improved breakdown characteristics of these RESURF devices are achieved by employing thinner but more highly doped epitaxial layers to reduce surface fields. As defined in my U.S. Pat. No. 4,300,150, the RESURF principle requires that appropriate values for the product of layer thickness and resistivity be selected. More particularly, the product of doping concentration and layer thickness for RESURF is defined in my prior patent as typically approximately 10^{12} atoms/cm^2, with a representative value of $1.8(10)^{12}$ atoms/cm^2 shown in the examples.

The RESURF technique was applied to lateral double-diffused MOS transistors, as reported in "Lateral DMOS Power Transistor Design", "IEEE Electron Device Letters", Vol. EDL-1, pages 51–53, April, 1980, by Colak et al and my U.S. Pat. No. 4,300,150, and the result was a substantial improvement in device characteristics. It should be understood that in high-voltage DMOS devices, there is always a trade-off between breakdown voltage, on-resistance and device size, with the goal being to increase the breakdown voltage level while maintaining a relatively low on-resistance in a relatively compact device. Using the prior art RESURF technique, and for reference assuming a constant breakdown voltage of about 400 volts, a very substantial improvement (e.g. decrease) in on-resistance may be obtained in a device of the same size as a conventional (thick epitaxial layer) DMOS device.

However, such prior art RESURF devices, with their thin epitaxial layers, are not suitable for use in source-follower applications or other circuit arrangements where both the source and drain are at a high potential with respect to the substrate. For such applications, these devices would require a substantially thicker epitaxial surface layer, thus negating a principal advantage of the RESURF technique and increasing device size and cost, or they would require a lower epitaxial doping level, which would increase on-resistance, again negating a principal advantage of the RESURF technique.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a lateral double-diffused MOS transistor which is suitable for use in source-follower applications or other circuit arrangements where both the source and drain are at a high potential with respect to the substrate.

It is a further object of the invention to provide a lateral double-diffused MOS transistor suitable for source-follower applications while maintaining the advantages of devices constructed using the RESURF technique.

In accordance with the invention, these objectives are achieved by a lateral double-diffused MOS transistor of the type described above, in which the single prior-art surface layer on the semiconductor substrate is replaced by a 3-layer configuration including a first semiconductor layer of the second conductivity type on the substrate, a second semiconductor layer of the first conductivity type on the first layer, and a third semiconductor surface layer of the second conductivity type on the second layer. This 3-layer configuration permits operation in the source-follower mode by preventing device breakdown when both the source and drain are operated at relatively high voltages with respect to the substrate.

In a further embodiment of the invention, a plurality of spaced-apart semiconductor zones of the second conductivity type are located within that portion of the second semiconductor layer extending from adjacent the channel region to beneath the drain contact region. These semiconductor zones may either be strip-shaped zones which extend continuously from adjacent the channel region to beneath the drain contact region or else each zone may include first and second subzones, with the first subzone located adjacent to the channel region and the second subzone spaced apart from the first subzone and located beneath the drain contact region of the device. These semiconductor zones serve to prevent the first semiconductor layer from floating by connecting it to the third semiconductor surface layer of the device, and also provide an additional RE-

SURF effect in the lateral direction, thus improving both breakdown voltage and device conductivity.

In another embodiment of the invention, device conductivity can be further improved by providing a second drain region and a further gate electrode, so that the second semiconductor layer can also contribute to device conductivity when the transistor is in the "on" state.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a vertical cross-sectional view of a lateral double-diffused MOS transistor in accordance with a first embodiment of the invention;

FIG. 2A is a plan view along the section line II—II of the transistor of FIG. 1;

FIG. 2B is a plan view of a lateral double-diffused MOS transistor in accordance with a second embodiment of the invention;

FIG. 2C is a plan view of a lateral double-diffused MOS transistor in accordance with a third embodiment of the invention; and

FIG. 3 is a vertical cross-sectional view of a lateral double-diffused MOS transistor in accordance with a fourth embodiment of the invention.

DETAILED DESCRIPTION

As noted above, conventional lateral double-diffused MOS transistors are not suitable for efficient use in source-follower circuits, because of the relatively thick epitaxial layers required to avoid punchthrough breakdown in the source-follower mode. This results in an unduly large and expensive-to-manufacture device. Furthermore, prior-art RESURF techniques, which permit the use of thinner epitaxial layers, result in devices which are unsuited for source-follower applications because of similar high-voltage breakdown problems. More specifically, in typical source-follower applications, the device substrate is normally grounded, while the drain, source and channel regions of the device experience high voltage levels in the "on" state when these devices are operated with high power supply voltages. Under such condition, conventional RESURF devices are subject to punchthrough breakdown (from channel to substrate) which precludes operation in the source-follower mode.

These prior-art problems are overcome in the present invention by a device such as that shown in FIG. 1, employing a triple-layer structure above the substrate. It should be noted that FIG. 1, as well as the remaining figures of the drawing, are not drawn to scale, and in particular the vertical dimensions are exaggerated for improved clarity. Additionally, like parts are designated with like reference numerals in the various figures, and semiconductor regions of the same conductivity type are shown hatched in the same direction.

In FIG. 1, a lateral double-diffused MOS transistor 10 has a semiconductor substrate 12 of a first conductivity type, here p-type, on which the device is constructed. A first semiconductor layer 14 of a second conductivity type opposite to that of the first, here n-type, is located on a first major surface 12*a* of the substrate, while a second semiconductor layer 16 of the first conductivity type is located on the first semiconductor layer. The basic layered construction of the device is completed by a third semiconductor surface layer 18 of the second conductivity type which is located on the second layer.

The lateral double-diffused MOS transistor of the invention is constructed within this layered structure by providing a first surface-adjoining channel region 20 of p-type material in the third layer, with a surface-adjoining source region 22 of n-type material in a portion of p-type region 20. A first surface-adjoining drain contact region 24 of n-type material is provided in the third layer 18 and is spaced apart from the first channel region, and a portion of the third semiconductor surface layer 18 between the drain contact region 24 and the first channel region 20 forms an extended drain region 24*a*. Similarly, that portion of the second layer extending from the channel region 20 to beneath the first drain contact region 24 forms an extended channel region.

An insulating layer 26 is provided on the surface of the transistor, over the third surface layer, and covers at least the portion of the first channel region 20 which is located between the source and the first drain regions. A first gate electrode 30 is provided on the insulating layer 26, over the previously-mentioned portion of the first channel region, and is electrically isolated from the third layer by the insulating layer 26. An electrical connection to the first drain contact region 24 is provided by a first drain electrode 32, while a source electrode 28 is provided to contact the source region 22, and this source electrode also serves to connect the first channel region 20 to the source region 22. The basic construction of the device is completed by a substrate electrode 34 on lower major surface 12*b* of the substrate 12.

The principal difference between the present invention and prior-art lateral double-diffused MOS transistors, such as FIG. 1 of my U.S. Pat. No. 4,300,150, lies in the presence of the second semiconductor layer 16, which in FIG. 1 forms a p-type extension of the channel region 20 between the n-type first and third semiconductor layers, and which extends from the channel region 20 to beneath the drain region 24, 24*a*. This configuration is in contrast to the prior art device shown in FIG. 1 of my prior patent, in which the area between the channel and drain is composed of a single n-type layer 12.

The three-layer configuration of my present invention affords several important design advantages, which permit the use of devices incorporating the present invention in source-follower circuits. In particular, by providing an extended channel in the form of second semiconductor layer 16, it is possible to increase the doping levels of the n-type first and third semiconductor layers to substantially avoid the channel-to-substrate punchthrough breakdown problem previously described. Ordinarily, such an increased doping level would be undesirable because it would reduce the drain-to-channel avalanche breakdown voltage of the device, but here, by adding the p-type second semiconductor layer, this undesirable decrease in avalanche breakdown voltage is substantially avoided. By redistributing the electrical field over a greater area of the device, the p-type second semiconductor layer utilizes the basic RESURF principle to reduce the localized magnitude of the electrical field adjacent the channel, and thus prevents avalanche breakdown in this region when higher doping levels are used in the third, and particularly the first, semiconductor layers in order to prevent punchthrough during operation in the source-follower mode. Thus, the present invention results in a device which is particularly suitable for high-voltage operation in the source-follower mode due to its improved punchthrough and avalanche breakdown characteristics.

Furthermore, in accordance with basic RESURF principles, the three semiconductor layers are not only more highly-doped than in conventional devices, but are also substantially thinner, thus resulting in a smaller, less expensive and easier-to-manufacture device. Thus, while the total thickness of all three semiconductor layers (i.e. the total thickness between insulating layer 26 and the upper surface 12*a* of the substrate) may typically be about 6 microns in the present invention for a device capable of operating at 400 volts, the prior-art MOS structure of Pocha et al, described above, requires an epitaxial layer thickness of greater than 23 microns in order to achieve a punchthrough breakdown voltage of only 200 volts. In addition, the relatively high doping levels of the semiconductor layers in the present invention provide improved normalized "on" resistance despite the use of relatively thin semiconductor layers. Thus, the present invention serves to improve both breakdown voltage and normalized "on" resistance, thereby permitting effective and efficient operation in the source-follower mode.

While the configuration of the present invention can be advantageously used in various device constructions, the following table of approximate values will illustrate the configuration of a typical device having a breakdown voltage of about 400 volts:

REGION (Ref. No.)	TYPE	TYPICAL DOPING	TYPICAL THICKNESS
First semiconductor layer (14)	n+	10^{16} donors/cm^3	2 microns
Second semiconductor layer (16)	p+	10^{16} acceptors/cm^3	2 microns
Third semiconductor layer (18)	n+	10^{16} donors/cm^3	2 microns
Source (22)	n++	10^{18}–10^{20} donors/cm^3	2 microns
Drain Contact (24)	n++	10^{18}–10^{20} donors/cm^3	2 microns
Channel (20)	p++	10^{17}–10^{20} acceptors/cm^3	4 microns
Substrate (12)	p−	10^{14}–10^{15} acceptors/cm^3	—

As can be seen from the above table, the product of doping concentration and layer thickness for the first, second and third layers is typically about $2(10)^{12}$ atoms/cm^2, in accordance with the RESURF principle.

A plan view of the device of FIG. 1 along the section line II—II is shown in FIG. 2A. This plan view shows a horizontal section of the p-type second semiconductor layer 16, as well as a portion of the more highly-doped channel region 20 which extends into the second semiconductor layer beneath the source. Due to the substantially continuous nature of this intermediate p-type layer between the upper (third) and lower (first) semiconductor layers, the lower n-type semiconductor layer does not conduct a portion of the total device current in the "on" state because layer 14 is isolated from the current-carrying path due to the intervening second semiconductor layer 16. However, substantial further reduction in normalized "on" resistance could be attained if the first semiconductor layer 16 of FIG. 2A were to be used as an additional current path. Two alternate embodiments for accomplishing this function are shown in FIGS. 2B and 2C.

In these embodiments, a plurality of spaced-apart semiconductor zones 16*c*, 16*d* of the second conductivity type (here n-type) are located within that portion of the second semiconductor layer 16 extending from adjacent the channel region 20 to beneath the drain contact region 24. In FIG. 2B, these semiconductor zones are formed from strip-shaped zones 16*c* which extend continuously from adjacent the channel region to beneath the drain contact region, while in FIG. 2C, each spaced-apart semiconductor zone is formed from a first sub-zone 16*d* located adjacent the channel region and a second sub-zone 16*d*′ which is spaced apart from the first sub-zone and is located beneath the drain contact region. These spaced-apart semiconductor zones 16*c*, 16*d* and 16*d*′ are n-type zones having a typical doping level of about 10^{16} donors/cm^3. In FIG. 2B, the lateral extent of the semiconductor zones 16*c* is shown by reference numerals 16*a* and 16*b* to denote the left and right edges, respectively, of the zones. In FIG. 1, dotted lines are used to show where these left and right edges would appear in a cross-section along the line I—I of FIG. 2B if these semiconductor zones were to be incorporated into the device of FIG. 1. As shown in FIG. 1, the semiconductor zones extend in the vertical direction from the third semiconductor layer 18 down to the first semiconductor layer 14.

By means of these semiconductor zones, a connection is formed between the upper (third) and lower (first) semiconductor layers, so that the first semiconductor layer is no longer floating, and can contribute to device conductivity in the "on" state, thus lowering normalized "on" resistance. In fact, normalized "on" resistance will be reduced by a factor of about 2 by including these semiconductor zones in the embodiment of FIG. 1. Additionally, by preventing the lower (first) semiconductor layer from floating by connecting it to the uppermost (third) semiconductor layer, an additional advantage is obtained in that the avalanche breakdown voltage of the device will be increased. Furthermore, with these zones, the critical nature of the upper (third) semiconductor layer decreases, so that it can be made thinner.

An additional embodiment of the invention, in which device conductivity is further improved, is shown in FIG. 3. This device differs from the device shown in FIG. 1 basically in that the single gate and drain structure of FIG. 1 is replaced by a modified dual-gate/dual-drain structure. More particularly, lateral double-diffused MOS transistor 11 includes a second surface-adjoining drain end region 40 of p-type material, as well as a second surface-adjoining channel region 36 of n-type material which is controlled by a further gate electrode 46 (G2) located over the second channel region. The embodiment of FIG. 3 also differs from the previously-described embodiment of FIG. 1 in that the original drain contact region 24 (hereinafter referred to as the first drain contact region for clarity) now includes a p-type surface region 38 within the n-type region 36, so that region 36 now also serves as a second surface-adjoining channel region for the new portion (on its right side), while the p-type zone 38 serves as a further surface-adjoining source region for the new portion of the device. A first drain electrode 44 contacts both source region 38 and region 36, and now serves as both a drain electrode (D1) for the original portion of the device and as a source electrode (S2) for the new portion. The purpose of this more complex dual-gate/dual-drain structure is to enhance device conductivity in the "on" state by enabling the second p-type semiconductor layer 16 to also contribute to device conductivity by conducting holes from region 38, through the second

channel region 36, the second drain end region 40 and the second semiconductor layer 16 back to source region 22. Electrode 28, which contacts both regions 20 and 22, now serves as both a source electrode (S1) for the original portion of the device and as a drain electrode (D2) for the new portion.

Yet a further improvement in normalized "on" resistance may be achieved by combining the dual-gate/dual-drain structure of FIG. 3 with the spaced-apart semiconductor zones 16c or 16d/d' of FIG. 2B or 2C. In this manner all three semiconductor layers will contribute to device conductivity, thus achieving optimum normalized "on" resistance.

Thus, by using a unique triple-layer construction, the present invention provides a lateral double-diffused MOS transistor which is capable of operating at high voltages in the source-follower mode, while at the same time providing a low normalized "on" resistance in a vertically compact and easily manufactured structure.

Finally, while the invention has been particularly shown and described with reference to certain preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made without departing from the spirit and scope of the invention.

I claim:

1. A lateral double-diffused MOS transistor, which comprises:

a semiconductor substrate of a first conductivity type;

a first semiconductor layer of a second conductivity type opposite to that of the first on a first major surface of said substrate;

a second semiconductor layer of said first conductivity type on said first layer;

a third semiconductor surface layer of said second conductivity type on said second layer, the product of the net doping concentration and the thickness of said first, second and third semiconductor layers each being selected to accordance with the RESURF principle such that the product of doping concentration and layer thickness is typically approximately 10^{12} atoms/cm^2;

a first surface-adjoining channel region of said first conductivity type in said third layer and connected to said second semiconductor layer;

a surface-adjoining source region of said second conductivity type in said channel region;

a first surface-adjoining drain contact region of said second conductivity type in said third layer and spaced apart from said first channel region;

an extended drain region formed from a portion of said third layer between said first drain contact region and said first channel region;

an insulating layer on the surface of said transistor and covering at least that portion of the first surface-adjoining channel region located between said source and said extended drain regions;

a first gate electrode on said insulating layer, over said portion of the first channel region and electrically isolated from said third layer; and

source and first drain electrodes connected respectively to the source and first drain contact regions of the transistor.

2. A lateral double-diffused MOS transistor as in claim 1, wherein the doping level of said second layer is higher than that of said substrate, the doping level of said first channel region is higher than that of said second layer, and the doping level of said source and first drain contact regions is higher than the doping level of said first and third layers.

3. A lateral double-diffused MOS transistor as in claim 2, wherein said source electrode electrically connects said source and first channel regions together, and further comprising a substrate electrode on a second major surface of said substrate opposite said first major surface.

4. A lateral double-diffused MOS transistor as in claim 1, further comprising a plurality of spaced-apart semiconductor zones of said second conductivity type located in that portion of said second semiconductor layer extending laterally from adjacent said first channel region to beneath said first drain contact region, said semiconductor zones extending vertically from said first semiconductor layer to said third semiconductor layer.

5. A lateral double-diffused MOS transistor as claimed in claim 4, wherein said spaced-apart zones comprise strip-shaped zones extending continuously from adjacent said first channel region to beneath said first drain contact region.

6. A lateral double-diffused MOS transistor as claimed in claim 4, wherein each of said spaced-apart zones comprises a first subzone located adjacent said first channel region and a second subzone, spaced apart from said first subzone and located beneath said first drain contact region.

7. A lateral double-diffused MOS transistor as claimed in claim 4, wherein said spaced-apart semiconductor zones comprise n-type zones having a doping level of about 10^{16} donors/cm^3.

8. A lateral double-diffused MOS transistor as in claim 1, further comprising a second surface-adjoining drain end region of said first conductivity type in said third layer, extending down to said first layer, and electrically isolated from said first drain contact region by a p-n junction, a second surface-adjoining channel region of said second conductivity type between said first drain contact region and said second drain end region, said insulating layer on the surface of said transistor further covering that portion of the second surface-adjoining channel region located between said drain regions, a further surface-adjoining source region of said first conductivity type in said second surface-adjoining channel region and connected to said first drain electrode, and a further gate electrode on said insulating layer, over said portion of the second channel region and electrically isolated from said third layer.

9. A lateral double-diffused MOS transistor as in claim 8, further comprising a plurality of spaced-apart semiconductor zones of said second conductivity type located in that portion of said second semiconductor layer extending laterally from adjacent said first channel region to at least beneath said first drain contact region, said semiconductor zones extending vertically from said first semiconductor layer to said third semiconductor layer.

10. A lateral double-diffused MOS transistor as claimed in claim 9, wherein said spaced-apart zones comprise strip-shaped zones extending continuously from adjacent said first channel region to at least beneath said first drain contact region.

11. A lateral double-diffused MOS transistor as claimed in claim 9, wherein each of said spaced-apart zones comprises a first subzone located adjacent said first channel region and a second subzone, spaced apart

from said first subzone and located beneath said first drain contact region.

12. A lateral double-diffused MOS transistor as in claim 1, wherein said first and third semiconductor layers comprise n-type layers having a doping level of about 10^{16} donors/cm^3. and a thickness of about 2 microns, and said second semiconductor layer comprises a p-type layer having a doping level of about 10^{16} acceptors/cm^3 and a thickness of about 2 microns.

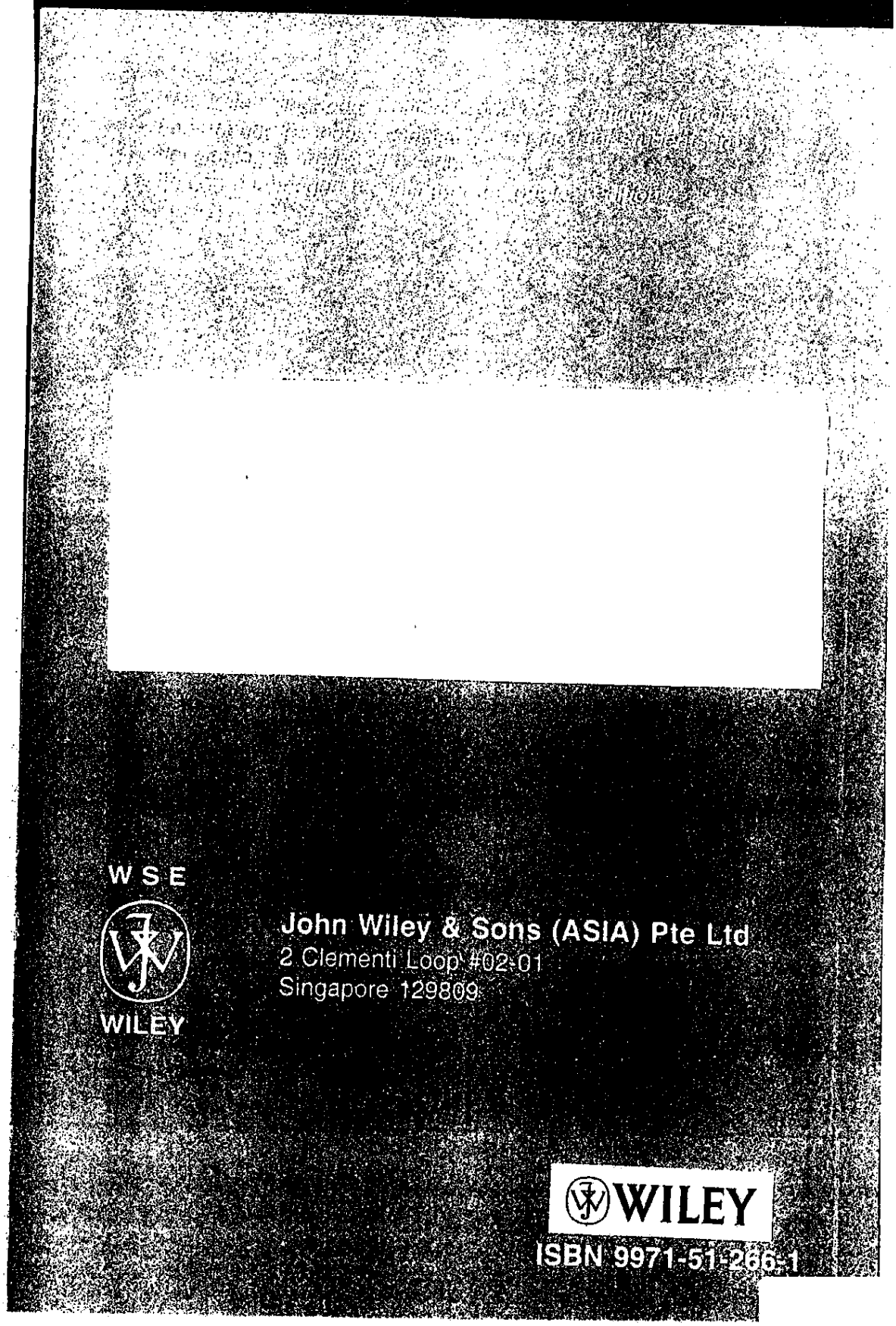
* * * * *

EXHIBIT K

Physics of Semiconductor Devices

2nd Edition

S.M. Sze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8

MOSFET

- INTRODUCTION
- BASIC DEVICE CHARACTERISTICS
- NONUNIFORM DOPING AND BURIED-CHANNEL DEVICES
- SHORT-CHANNEL EFFECTS
- MOSFET STRUCTURES
- NONVOLATILE MEMORY DEVICES

8.1 INTRODUCTION

The metal–oxide–semiconductor field-effect transistor (MOSFET) is the most important device for very-large-scale integrated circuits such as microprocessors and semiconductor memories. MOSFET is also becoming an important power device. It has many acronyms including IGFET (insulated-gate field-effect transistor) MISFET (metal–insulator–semiconductor field-effect transistor) and MOST (metal–oxide–semiconductor transistor). The principle of the surface field-effect transistor was first proposed in the early 1930s by Lilienfeld[1] and Heil.[2] It was subsequently studied by Shockley and Pearson[3] in the late 1940s. In 1960, Kahng and Atalla[4] proposed and fabricated the first MOSFET using a thermally oxidized silicon structure. The basic device characteristics have been subsequently studied by Ihantola and Moll,[5,6] Sah,[7] and Hofstein and Heiman.[8] The technology, application, and device physics have been reviewed by Wallmark and Johnson,[9] Richman,[10] and Brews.[11]

Because the current in a MOSFET is transported predominantly by carriers of one polarity only (e.g., electrons in an n-channel device), the MOSFET is usually referred to as a unipolar device. The MOSFET is a member of the family of field-effect transistors. The other members, JFETs and MESFETs, have already been considered in Chapter 6. Al-

though MOSFETs have been made with various semiconductors such as Ge,[12] Si, and GaAs,[13] and use various insulators such as SiO_2, Si_3N_4, and Al_2O_3, the most important system is the Si–SiO_2 combination. Hence most of the results in this chapter are obtained from the Si–SiO_2 system.

We first consider the basic device characteristics of the so-called long-channel MOSFET; that is, the channel length L is much longer than the sum of the source and drain depletion-layer widths ($W_S + W_D$).* This serves as a foundation to understand short-channel, that is, $L \lesssim (W_S + W_D)$, and related MOSFET devices.

Figure 1 shows[14] the reduction of the minimum device dimension since the beginning of the integrated circuit era in 1959. Figure 1 also shows that the minimum dimension will shrink continuously; the 1-μm barrier for commercial devices may be overcome by 1990. The reduction of device dimensions is driven by the requirement that integrated circuits of high complexity be fabricated. The number of components per integrated-circuit

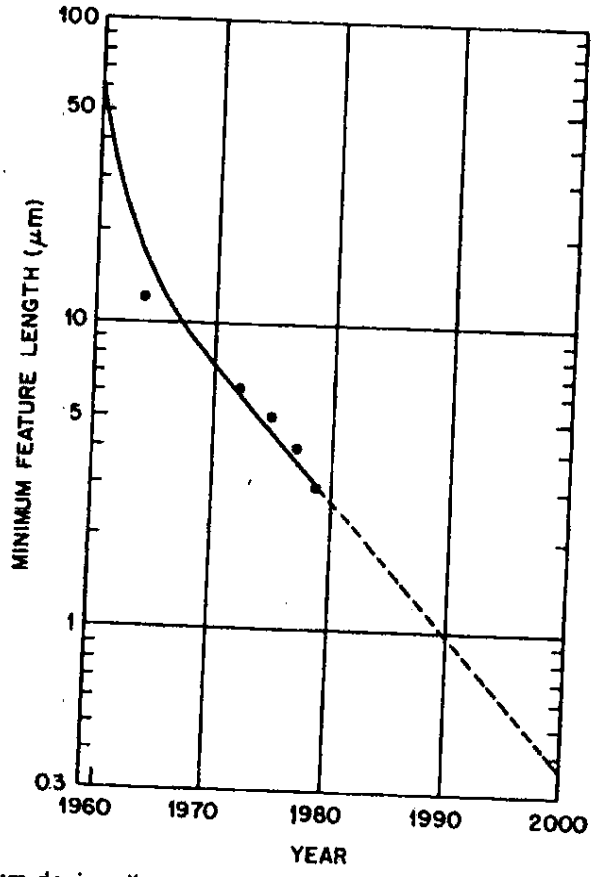

Fig. 1 The minimum device dimension in an integrated circuit as a function of the year for commercial devices. (After Ref. 14.)

*These terms will be defined in Section 8.2.

Fig. 2

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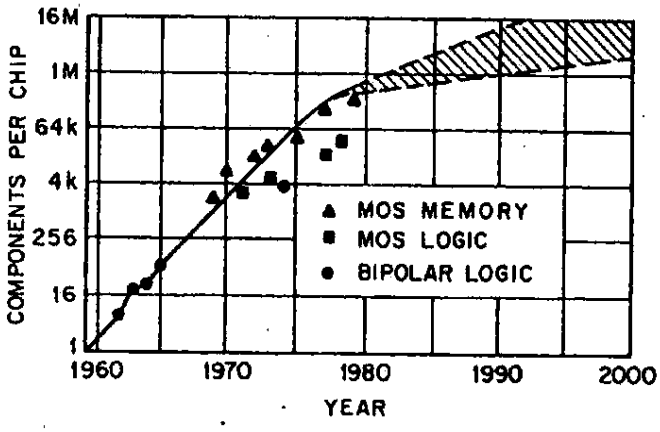

Fig. 2 Complexity of integrated circuits as a function of the year. (After Moore, Ref. 15.)

chip has grown exponentially[15] since 1959 (Fig. 2). The rate of growth is expected to slow down because of a lack of product definition and design. However, a complexity of 1 million or more devices per chip may be available around 1990 using 1-μm or submicron device geometries. As the channel length becomes shorter, one has to consider short-channel effects due to two-dimensional potential, high-field transport and oxide charging. Many device structures have been proposed to improve MOSFET performance. Some representative structures as well as the nonvolatile semiconductor memory, basically a MOSFET with a multilayer gate structure, will be discussed.

8.2 BASIC DEVICE CHARACTERISTICS

The basic structure of a metal–oxide–semiconductor field-effect transistor (MOSFET) is illustrated in Fig. 3. It is a four-terminal device and consists of a p-type semiconductor substrate into which two n^+ regions, the source and drain, are formed* (e.g., by ion implantation). The metal contact on the insulator is called gate; heavily doped polysilicon or a combination of silicide and polysilicon can also be used as the gate electrode. The basic device parameters are the channel length L, which is the distance between the two metallurgical n^+-p junctions; the channel width Z; the insulator thickness d; the junction depth r_j; and the substrate doping N_A. In a silicon integrated circuit, a MOSFET is surrounded by a thick oxide (called the field oxide to distinguish it from the gate oxide) to isolate it from adjacent devices.

The source contact will be used as the voltage reference throughout this

*This is an n-channel device; one may consider a p-channel device by exchanging p for n and reversing the polarity of the voltage.

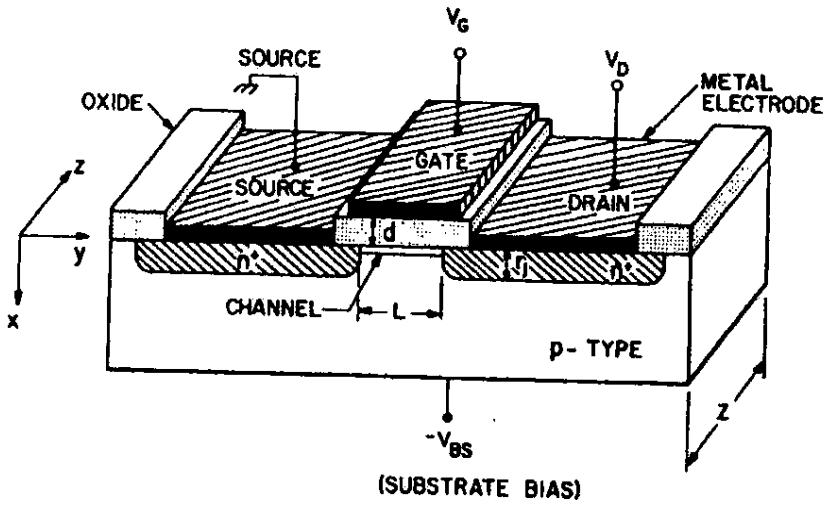

Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)

chapter. When no voltage is applied to the gate, the source-to-drain electrodes correspond to two p-n junctions connected back to back. The only current that can flow from source to drain is the reverse leakage current.* When a sufficiently large positive bias is applied to the gate so that a surface inversion layer (or channel) is formed between the two n^+ regions, the source and the drain are then connected by a conducting-surface n channel through which a large current can flow. The conductance of this channel can be modulated by varying the gate voltage. The back-surface contact (or substrate contact) can have the reference voltage or be reverse-biased; the back-surface voltage will also affect the channel conductance.

8.2.1 Nonequilibrium Condition

When a voltage is applied across the source–drain contacts, the MOS structure is in a nonequilibrium condition; that is, the imref of the minority carriers (electrons, in the present case) is lowered from the equilibrium Fermi level. To show more clearly the band bending across the device, Fig. 4*a* shows[16] the MOSFET turned 90°. The two-dimensional, flat-band, zero-bias ($V_G = V_D = V_{BS} = 0$) equilibrium condition is shown in Fig. 4*b*. The equilibrium conditions under a gate bias that causes surface inversion are shown in Fig. 4*c*. The nonequilibrium condition with both drain and gate biases is shown in Fig. 4*d*, where we note the separation of the imrefs of electrons and holes; the hole imref E_{Fp} remains at the bulk Fermi level while the electron imref E_{Fn} (minority in the present case) is lowered

*This is the n-channel normally-off (enhancement-type) MOSFET. Other types will be discussed later.

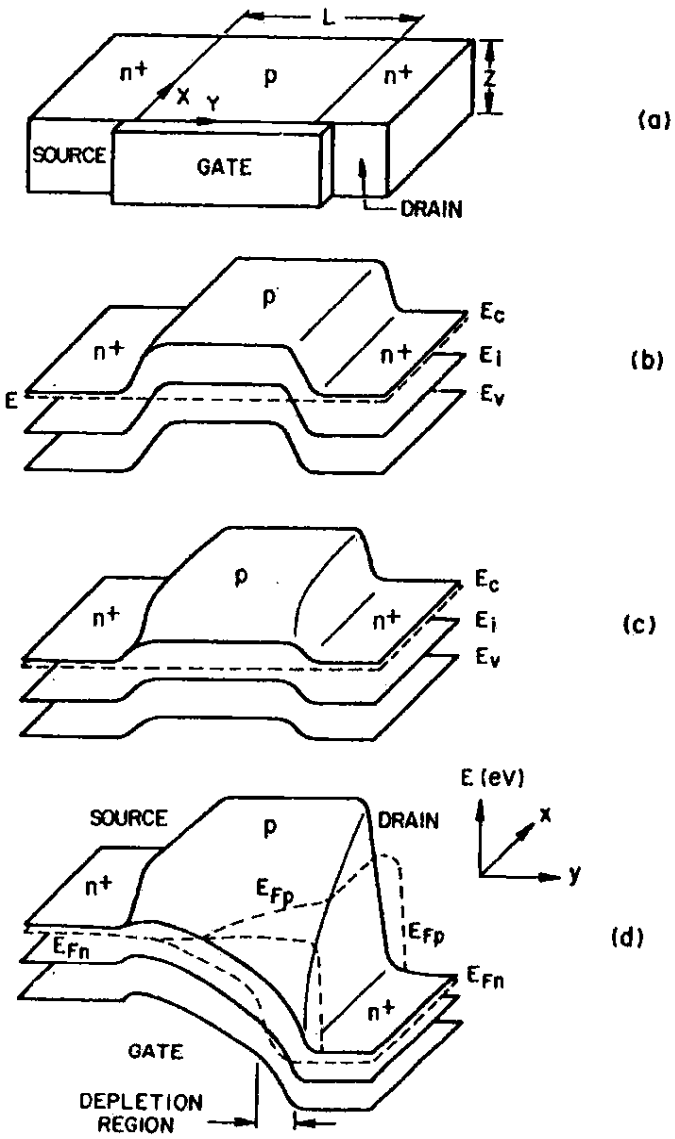

Fig. 4 Two-dimensional band diagram of an *n*-channel MOSFET. (a) Device configuration. (*b*) Flat-band zero-bias equilibrium condition. (*c*) Equilibrium condition under a gate bias. (*d*) Nonequilibrium condition under both gate and drain biases. (After Pao and Sah, Ref. 16.)

toward the drain contact. Figure 4*d* shows that the gate voltage required for inversion at the drain is larger than the equilibrium case in which $\psi_s(\text{inv}) \simeq 2\psi_B$. This is because the applied drain bias lowers the electron imref, and an inversion layer can be formed only when the potential at the surface crosses over the imref of the minority carrier.

Figure 5 shows a comparison[17] of the charge distribution and energy-band variation of an inverted *p* region for the equilibrium case and the nonequilibrium case at the drain. For the equilibrium case (discussed in Chapter 7), the surface depletion region reaches a maximum width W_m at

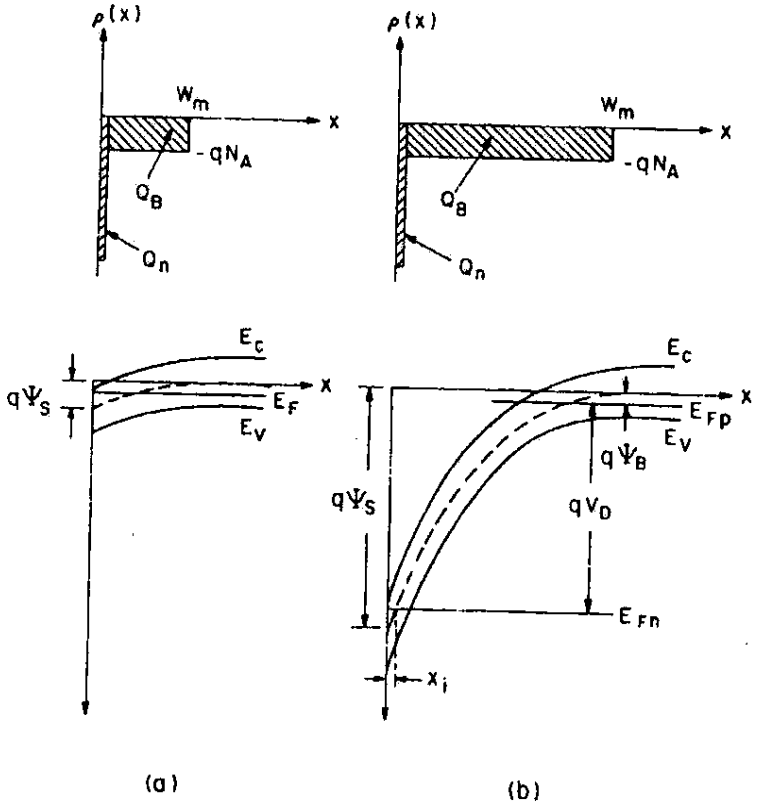

Fig. 5 Comparison of charge distribution and energy band variation of an inverted p region for (a) the equilibrium case and (b) the nonequilibrium case at the drain. (After Grove and Fitzgerald, Ref. 17.)

inversion. For the nonequilibrium case, the depletion-layer width is a function of the bias V_D, and the surface potential ψ_s at the onset of strong inversion is given, to a good approximation, by

$$\psi_s(\text{inv}) \simeq V_D + 2\psi_B . \tag{1}$$

The derivation for the characteristic of the surface-space charge under the nonequilibrium condition is similar to that in Chapter 7. The two assumptions are that (1) the imref for the majority carriers of the substrate does not vary with distance from the bulk to the surface, and (2) the imref for the minority carriers of the substrate is separated by the applied junction bias V_D from the imref for the majority carriers; that is, $E_{Fp} = E_{Fn} + qV_D$ for a p substrate. The first assumption introduces little error when the surface is inverted, because majority carriers are then only a negligible part of the surface space charge; the second assumption is correct under the inversion condition, because minority carriers are an important part of the surface-space-charge region when the surface is inverted.

Based on these assumptions, the one-dimensional Poisson equation for

the surface-space-charge region at the drain is given by

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\epsilon_s}(N_D^+ - N_A^- + p - n) \tag{2}$$

where

$$N_D^+ - N_A^- = n_{po} - p_{po}, \qquad p_{po} \simeq N_A$$
$$p = p_{po}e^{-\beta\psi}$$
$$n = n_{po}e^{\beta\psi - \beta V_D}, \qquad \beta \equiv q/kT. \tag{3}$$

Following the same approach as in Chapter 7, we obtain

$$\mathscr{E} = -\frac{\partial\psi}{\partial x} = \pm\frac{\sqrt{2}kT}{qL_D}F\left(\beta\psi, V_D, \frac{n_{po}}{p_{po}}\right) \tag{4}$$

and

$$Q_s = -\epsilon_s\mathscr{E}_s = \mp\frac{\sqrt{2}\epsilon_s kT}{qL_D}F\left(\beta\psi_s, V_D, \frac{n_{po}}{p_{po}}\right) \tag{5}$$

where

$$F\left(\beta\psi, V_D, \frac{n_{po}}{p_{po}}\right) \equiv \left[e^{-\beta\psi} + \beta\psi - 1 + \frac{n_{po}}{p_{po}}e^{-\beta V_D}(e^{\beta\psi} - \beta\psi e^{\beta V_D} - 1)\right]^{1/2} \tag{6}$$

and

$$L_D \equiv \left(\frac{kT\epsilon_s}{p_{po}q^2}\right)^{1/2}. \tag{7}$$

The surface charge per unit area after strong inversion is given by

$$Q_s = Q_n + Q_B \tag{8}$$

where

$$Q_B = -qN_AW_m = -\sqrt{2qN_A\epsilon_s(V_D + 2\psi_B)} \tag{9}$$

and Q_n, the charge due to minority carriers within the inversion layer, is

$$|Q_n| \equiv q\int_0^{x_i} n(x)\,dx = q\int_{\psi_s}^{\psi_B}\frac{n(\psi)\,d\psi}{d\psi/dx} \tag{10}$$

or

$$|Q_n| = q\int_{\psi_s}^{\psi_B}\frac{n_{po}e^{(\beta\psi - \beta V_D)}\,d\psi}{(\sqrt{2}kT/qL_D)F(\beta\psi, V_D, n_{po}/p_{po})} \tag{11}$$

where x_i denotes the point at which the intrinsic Fermi level intersects the imref for electrons. For the practical doping ranges in silicon, the value of x_i is quite small, of the order of 30 to 300 Å. Equation 11 is the basic formula for long-channel MOSFET, and can be evaluated numerically.

Under strong inversion conditions, a simplified expression for Q_n can be obtained from a charge-sheet model[18] and is given by

$$|Q_n| = \sqrt{2}qN_A L_D \left\{ \left[\beta\psi_s + \left(\frac{n_{po}}{p_{po}}\right) e^{(\beta\psi_s - \beta V_D)} \right]^{1/2} - (\beta\psi_s)^{1/2} \right\}. \quad (12)$$

This expression for Q_n is derived under the condition $V_{BS} = 0$. When a substrate reverse bias is applied, the depletion width increase, and the term βV_D in Eq. 12 is replaced by $\beta(V_D + V_{BS})$.

8.2.2 Linear and Saturation Regions

We shall first present a qualitative discussion of device operation. Let us consider that a voltage is applied to the gate, causing an inversion at the semiconductor surface, Fig. 6*a*. If a small drain voltage is applied, a current will flow from the source to the drain through the conducting channel. Thus the channel acts as a resistance, and the drain current I_D is proportional to the drain voltage V_D. This is the linear region. As the drain voltage increases, it eventually reaches a point at which the channel depth x_j at $y = L$ is reduced to zero; this is called the pinch-off point, Fig. 6*b*. Beyond the pinch-off point the drain current remains essentially the same, because for $V_D > V_{D\,sat}$, the voltage at Y remains the same, $V_{D\,sat}$. Thus the number of carriers arriving at point Y from the source, and hence the current flowing from source to drain, remains the same apart from a decrease in L to the value L' (Fig. 6*c*). Carrier injection from Y into the drain-depletion region is quite similar to the case of carrier injection from an emitter–base junction to the base–collector depletion region of a bipolar transistor.

We shall now derive the basic MOSFET characteristics under the following idealized conditions: (1) the gate structure corresponds to an ideal MOS diode as defined in Chapter 7; that is, there are no interface traps, fixed oxide charge, or work-function difference, and so on; (2) only drift current will be considered; (3) carrier mobility in the inversion layer is constant; (4) doping in the channel is uniform; (5) reverse leakage current is negligibly small; and (6) the transverse field ($\mathscr{E}_x$ in the x direction) in the channel is much larger than the longitudinal field ($\mathscr{E}_y$ in the y direction). The last condition corresponds to the so-called gradual channel approximation.

Under such idealized conditions, the total charge induced in the semiconductor per unit area Q_s at a distance y from the source is given by

$$Q_s(y) = [-V_G + \psi_s(y)]C_i \quad (13)$$

where $C_i \equiv \epsilon_i/d$ is the capacitance per unit area. The charge in the inversion layer is given by

$$\begin{aligned} Q_n(y) &= Q_s(y) - Q_B(y) \\ &= -[V_G - \psi_s(y)]C_i - Q_B(y). \end{aligned} \quad (14)$$

The surface potential $\psi_s(y)$ at inversion can be approximated by $2\psi_B +$

of device parameters. With other choices of device parameters, the relative importance of the various mechanisms changes.

To reduce the parasitic transistor effect, the resistance of the substrate R_{sub} can be minimized so that the product of the substrate current and R_{sub} remains smaller than 0.6 V when the drain voltage is equal to or larger than the corresponding BV_{CEO}. Then the breakdown voltage of a short-channel MOSFET will no longer be limited by BV_{CEO}; higher voltages and more reliable operation can be expected.[50] To reduce oxide charging, the density of water-related traps in the oxide should be minimized,[53] because such traps are known to capture electrons. To increase the punch-through voltage, single or double ion-implanted device structures can be made to increase the doping of the surface region. These structures will be considered in Section 8.5.

8.5 MOSFET STRUCTURES

Many device structures have been proposed to improve MOSFET performance with higher response speed, lower power consumption, more reliable operation, and higher power-handling capability. We shall now consider some representative structures.

8.5.1 Scaled-Down Device

In Section 8.4 we pointed out that short-channel effects are generally undesirable. One approach to avoid these effects is to maintain the long-channel behavior by simply scaling down all dimensions and voltages of a long-channel MOSFET, so that the internal electric fields are the same. This approach offers a conceptually simple picture for device miniaturization.

Figure 51*a* and *b* show the traditional large device and the scaled-down device,[54] respectively, in which all dimensions are shrunk by a "scaling factor," κ. This shrinking includes oxide thickness, channel length, channel width, and junction depth. The doping level is increased by κ, and all voltages are reduced by κ, leading to a reduction of the junction depletion width by about κ. Figure 51*c* compares I_D versus V_G in the linear region for the large and the scaled-down device. The threshold voltage is also reduced approximately by κ. Therefore, the number of devices per unit area increases by a factor of κ^2, the delay time due to transit across the channel, Eq. 54, decreases by κ, and the power dissipated per cell decreases by κ^2.

Note that in Fig. 51*c* the subthreshold current remains essentially the same for both devices. It remains the same because the subthreshold swing S, which is proportional to $(1 + C_D/C_i)$, remains the same as both capacitances are scaled up by the same factor κ. In addition, the junction

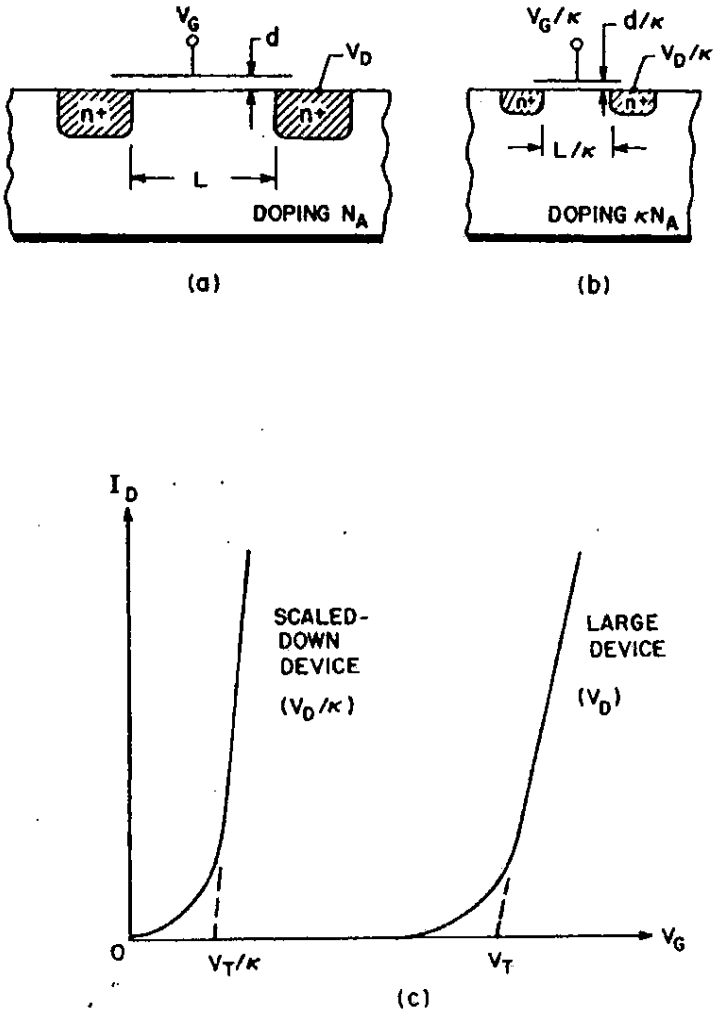

Fig. 51 Scaling approach for device miniaturization. (a) Long-channel device. (*b*) Scaled device. (*c*) Drain characteristics of these devices. (After Dennard et al., Ref. 54.)

built-in voltage and the surface potential for the onset of weak inversion do not scale (only ~10% change for 10 times increase in dopings). The range of gate voltage between depletion and heavy inversion is approximately 0.5 V. The parasitic capacitance may not scale, and the interconnect resistance increases when dimensions become smaller.

The expression for the minimum channel length, Eq. 83, can be used for a more flexible scaling approach.[41] For a given L_{min}, the value of γ is obtainable from Eq. 83, or Fig. 35, which allows the various device parameters to be adjusted independently as long as the value of γ remains the same. Therefore, all device parameters do not have to be scaled by the same factor κ. This flexibility allows one to choose new geometries that are easier to make or which optimize other aspects of device operation, rather than choosing strictly scaled geometries.

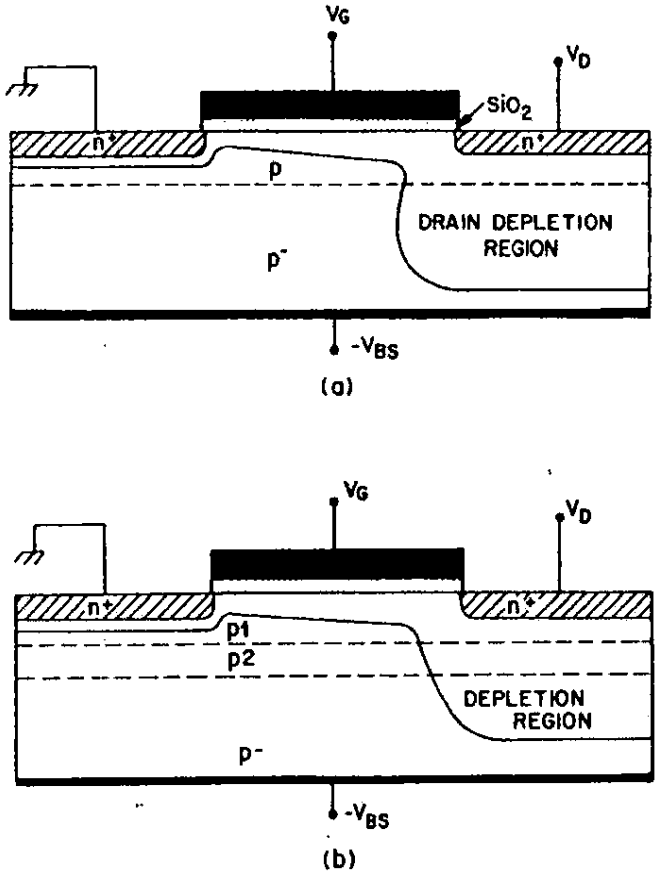

Fig. 52 HMOS structures. (a) Single implantation. (*b*) Double implantation. (After Shannon, Stephen, and Freeman, Ref. 55; Nihira et al., Ref. 56.)

8.5.2 HMOS

Figure 52 shows HMOS (high-performance MOS) structures. Figure 52*a* has a single ion implantation to increase the doping level at the surface region.[55] The implantation can control the threshold voltage and increase the punch-through voltage. Yet the surface region is shallow enough so that under operating conditions, the drain depletion-layer width extends into the low-doped substrate, reducing the drain capacitance. Figure 52*b* shows a double-implanted HMOS.[56] The $p1$ region contains the threshold control implant, and the $p2$ region contains the punch-through control implant. Using double implants, the HMOS with physical small-channel lengths can be tailored to minimize short-channel effects.

The implantations, however, degrade the subthreshold behavior[19] (large subthreshold swing) and can increase substrate bias sensitivity (becoming more sensitive to V_{BS}). However, various trade-offs exist and should be considered for device optimization.

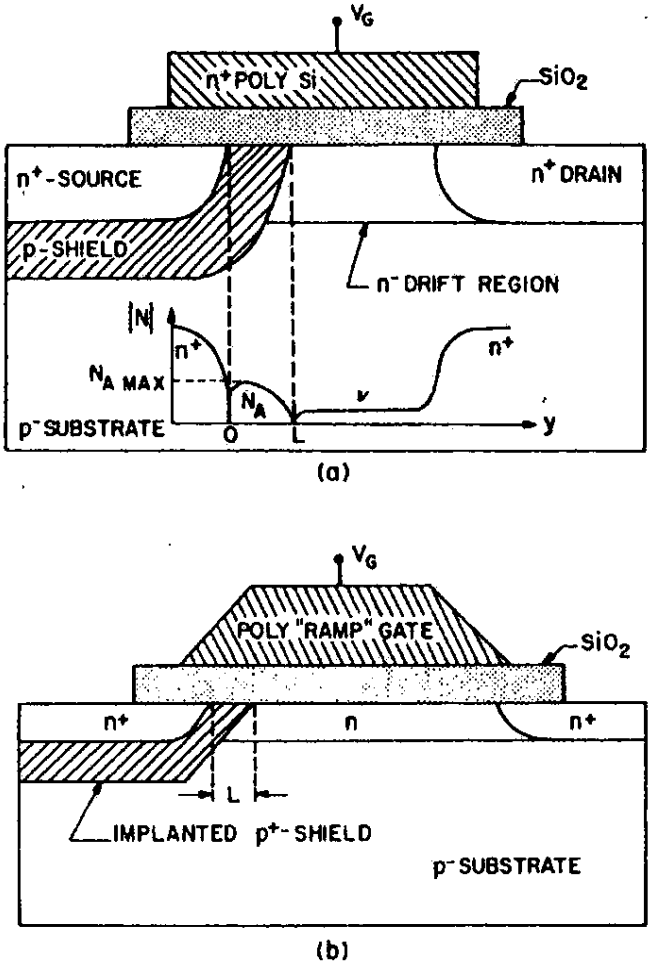

Fig. 53 (a) DMOS. (b) DIMOS structure. (After Tarui, Hayashi, and Sekigawa, Ref. 57; Tihanyi and Widmann, Ref. 58.)

8.5.3 DMOS

Figure 53*a* shows the DMOS (double-diffused MOS) structure,[57] where the channel length L is determined by the higher rate of diffusion of the p-dopant (e.g., boron), compared to the n^+-dopant (e.g., phosphorus) of the source. The channel is followed by a lightly doped drift region. Figure 53*a* also shows the doping profile along the semiconductor surface. Another version of DMOS is made by implantation. DIMOS (double-implanted MOS)[58] forms its source and drain by using a polysilicon gate as mask. The gate is tapered and the p^+-shield region is shaped by implantation through the tapered gate. The DIMOS structure improves the control in DMOS structures.

The DMOS and DIMOS structures can have very short channels and do not depend on a lithographic mask to determine channel length. Both

structures have good punch-through control because of the heavily doped p-shield. The lightly doped drift region minimizes the voltage drop across the region by maintaining a uniform field ($\geq 10^4$ V/cm) to achieve velocity saturation.[59] The field near the drain is the same as in the drift region, so avalanche breakdown, multiplication, and oxide charging are lessened, compared to conventional MOSFETs and HMOSs.[11]

However, the threshold voltage V_T is more difficult to control in DMOS.[60] As shown in Fig. 53*a*, V_T is determined by the maximum doping concentration $N_{A\,max}$ along the semiconductor surface. Varying $N_{A\,max}$ leads to variations in V_T. The localization of punch-through control to a thin p^+-shield region requires a higher doping level compared to HMOS, which leads to poorer turn-off behavior for DMOS.

8.5.4 Recessed-Channel MOSFET

The insert of Fig. 54 shows a MOSFET with a recessed channel.[61] The junction depth r_j for this structure is zero or negative. Figure 35 of Section 8.4 showed that the minimum channel length decreases as $r_j^{1/3}$. Figure 54 demonstrates that by reducing r_j, short-channel effects are minimized. For a given oxide thickness and substrate doping, as r_j decreases the onset of a large drop of V_T occurs at progressively shorter channels.

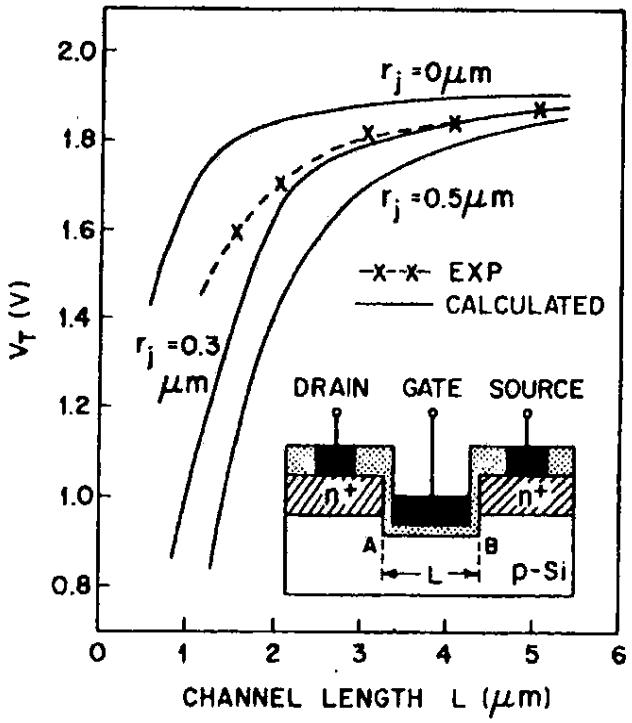

Fig. 54 Calculated and experimental V_T versus L plot for various junction depths. Insert shows a recessed-channel MOSFET. (After Nishimatsu et al., Ref. 61.)

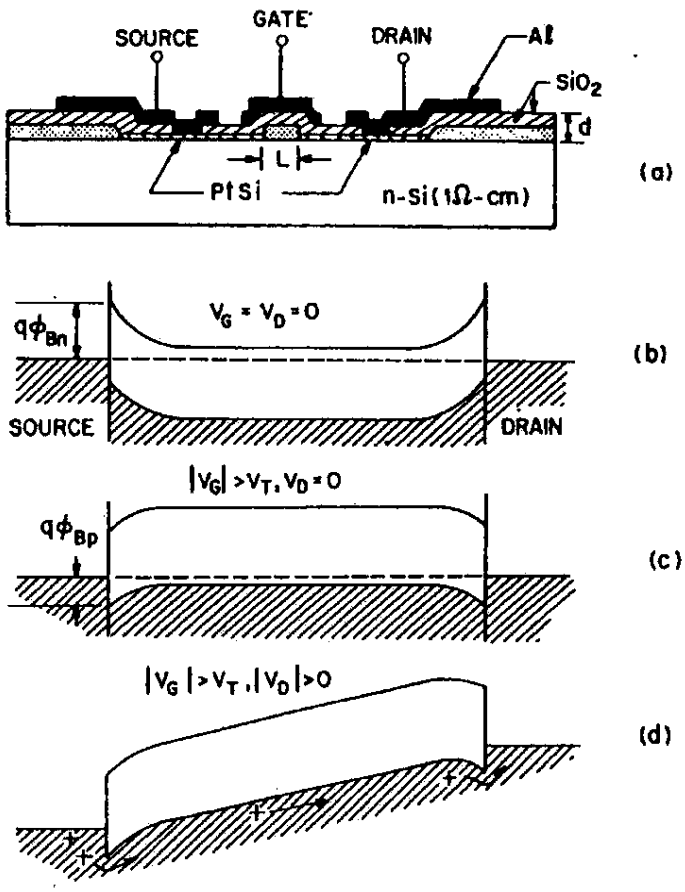

Fig. 55 MOSFET with Schottky-barrier source and drain. (a) Cross-sectional view of the device. (*b*), (*c*), and (*d*) Band diagrams for various biases. (After Lepselter and Sze, Ref. 62.)

The drawback of the recessed-channel structure, especially for submicron devices, is the difficulty in controlling the contour and the oxide thickness at corners A and B where the threshold voltage is determined. Also, oxide charging may be worsened, because more hot electron injection will occur.

8.5.5 Schottky-Barrier Source and Drain

Using Schottky-barrier contacts for the source and drain of a MOSFET results in performance and fabrication advantages. Figure 55*a* shows a schematic MOSFET structure with Schottky-barrier source and drain.[62] For a Schottky contact, the junction depth can effectively be made zero to minimize the short-channel effects. The high conductivity of the contact can also minimize source series resistance.

Eliminating high-temperature annealing steps can promote better quality in the oxides and better control of geometry. In addition, this structure can

EXHIBIT L

Manual of PATENT EXAMINING PROCEDURE

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Additions to the text of the Manual are indicated by arrows (><) inserted in the text. Deletions are indicated by a single asterisk (*) where a single word was deleted and by two asterisks (**) where more than one word was deleted. The use of three or five asterisks in the body of the laws, rules, treaties, and administrative instructions indicates a portion of the law, rule, treaty, or administrative instruction which was not reproduced.

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Revision 2, May 2004
Revision 3, August 2005
Revision 4, October 2005

(A) "R is halogen, for example, chlorine";

(B) "material such as rock wool or asbestos" *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1949);

(C) "lighter hydrocarbons, such, for example, as the vapors or gas produced" *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949); and

(D) "normal operating conditions such as while in the container of a proportioner" *Ex parte Steigerwald*, 131 USPQ 74 (Bd. App. 1961).

>The above examples of claim language which have been held to be indefinite are fact specific and should not be applied as *per se* rules. See MPEP § 2173.02 for guidance regarding when it is appropriate to make a rejection under 35 U.S.C. 112, second paragraph.<

2173.05(e) Lack of Antecedent Basis [R-1]

A claim is indefinite when it contains words or phrases whose meaning is unclear. The lack of clarity could arise where a claim refers to "said lever" or "the lever," where the claim contains no earlier recitation or limitation of a lever and where it would be unclear as to what element the limitation was making reference. Similarly, if two different levers are recited earlier in the claim, the recitation of "said lever" in the same or subsequent claim would be unclear where it is uncertain which of the two levers was intended. A claim which refers to "said aluminum lever," but recites only "a lever" earlier in the claim, is indefinite because it is uncertain as to the lever to which reference is made. Obviously, however, the failure to provide explicit antecedent basis for terms does not always render a claim indefinite. If the scope of a claim would be reasonably ascertainable by those skilled in the art, then the claim is not indefinite. *Ex parte Porter*, 25 USPQ2d 1144, 1145 (Bd. Pat. App. & Inter. 1992) ("controlled stream of fluid" provided reasonable antecedent basis for "the controlled fluid"). Inherent components of elements recited have antecedent basis in the recitation of the components themselves. For example, the limitation "the outer surface of said sphere" would not require an antecedent recitation that the sphere has an outer surface. >See *Bose Corp. v. JBL, Inc.*, 274 F.3d 1354, 1359, 61 USPQ2d 1216, 1218-19 (Fed. Cir 2001) (holding that recitation of "an ellipse" provided antecedent basis for "an ellipse having a major diameter" because "[t]here can be no dispute that mathematically an inherent characteristic of an ellipse is a major diameter").<

EXAMINER SHOULD SUGGEST CORRECTIONS TO ANTECEDENT PROBLEMS

Antecedent problems in the claims are typically drafting oversights that are easily corrected once they are brought to the attention of applicant. The examiner's task of making sure the claim language complies with the requirements of the statute should be carried out in a positive and constructive way, so that minor problems can be identified and easily corrected, and so that the major effort is expended on more substantive issues. However, even though indefiniteness in claim language is of semantic origin, it is not rendered unobjectionable simply because it could have been corrected. *In re Hammack*, 427 F.2d 1384 n.5, 166 USPQ 209 n.5 (CCPA 1970).

A CLAIM TERM WHICH HAS NO ANTECEDENT BASIS IN THE DISCLOSURE IS NOT NECESSARILY INDEFINITE

The mere fact that a term or phrase used in the claim has no antecedent basis in the specification disclosure does not mean, necessarily, that the term or phrase is indefinite. There is no requirement that the words in the claim must match those used in the specification disclosure. Applicants are given a great deal of latitude in how they choose to define their invention so long as the terms and phrases used define the invention with a reasonable degree of clarity and precision.

A CLAIM IS NOT *PER SE* INDEFINITE IF THE BODY OF THE CLAIM RECITES ADDITIONAL ELEMENTS WHICH DO NOT APPEAR IN THE PREAMBLE

The mere fact that the body of a claim recites additional elements which do not appear in the claim's preamble does not render the claim indefinite under 35 U.S.C. 112, second paragraph. See *In re Larsen*, No. 01-1092 (Fed. Cir. May 9, 2001) (unpublished) (The preamble of the *Larsen* claim recited only a hanger and a loop but the body of the claim positively recited a linear member. The examiner rejected the claim under 35 U.S.C. 112, second paragraph, because the omission from the claim's preamble of a critical element (i.e., a linear member) renders that

claim indefinite. The court reversed the examiner's rejection and stated that the totality of all the limitations of the claim and their interaction with each other must be considered to ascertain the inventor's contribution to the art. Upon review of the claim in its entirety, the court concluded that the claim at issue apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C. 112, paragraph 2.).

2173.05(f) Reference to Limitations in Another Claim

A claim which makes reference to a preceding claim to define a limitation is an acceptable claim construction which should not necessarily be rejected as improper or confusing under 35 U.S.C. 112, second paragraph. For example, claims which read: "The product produced by the method of claim 1." or "A method of producing ethanol comprising contacting amylose with the culture of claim 1 under the following conditions ....." are not indefinite under 35 U.S.C. 112, second paragraph, merely because of the reference to another claim. See also *Ex parte Porter*, 25 USPQ2d 1144 (Bd. Pat. App. & Inter. 1992) where reference to "the nozzle of claim 7" in a method claim was held to comply with 35 U.S.C. 112, second paragraph. However, where the format of making reference to limitations recited in another claim results in confusion, then a rejection would be proper under 35 U.S.C. 112, second paragraph.

2173.05(g) Functional Limitations [R-3]

A functional limitation is an attempt to define something by what it does, rather than by what it is (e.g., as evidenced by its specific structure or specific ingredients). There is nothing inherently wrong with defining some part of an invention in functional terms. Functional language does not, in and of itself, render a claim improper. *In re Swinehart*, 439 F.2d 210, 169 USPQ 226 (CCPA 1971).

A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. A functional limitation is often used in association with an element, ingredient, or step of a process to define a particular capability or purpose that is served by the recited element, ingredient or step. >In *Innova/Pure Water Inc. v. Safari Water Filtration Sys. Inc.*, 381 F.3d 1111, 1117-20, 72 USPQ2d 1001, 1006-08 (Fed. Cir. 2004), the court noted that the claim term "operatively connected" is "a general descriptive claim term frequently used in patent drafting to reflect a functional relationship between claimed components," that is, the term "means the claimed components must be connected in a way to perform a designated function." "In the absence of modifiers, general descriptive terms are typically construed as having their full meaning." *Id.* at 1118, 72 USPQ2d at 1006. In the patent claim at issue, "subject to any clear and unmistakable disavowal of claim scope, the term 'operatively connected' takes the full breath of its ordinary meaning, i.e., 'said tube [is] operatively connected to said cap' when the tube and cap are arranged in a manner capable of performing the function of filtering." *Id.* at 1120, 72 USPQ2d at 1008.<

Whether or not the functional limitation complies with 35 U.S.C. 112, second paragraph, is a different issue from whether the limitation is properly supported under 35 U.S.C. 112, first paragraph, or is distinguished over the prior art. A few examples are set forth below to illustrate situations where the issue of whether a functional limitation complies with 35 U.S.C. 112, second paragraph, was considered.

It was held that the limitation used to define a radical on a chemical compound as "incapable of forming a dye with said oxidizing developing agent" although functional, was perfectly acceptable because it set definite boundaries on the patent protection sought. *In re Barr*, 444 F.2d 588, 170 USPQ 33 (CCPA 1971).

In a claim that was directed to a kit of component parts capable of being assembled, the Court held that limitations such as "members adapted to be positioned" and "portions . . . being resiliently dilatable whereby said housing may be slidably positioned" serve to precisely define present structural attributes of interrelated component parts of the claimed assembly. *In re Venezia*, 530 F.2d 956, 189 USPQ 149 (CCPA 1976).

2173.05(h) Alternative Limitations

I. MARKUSH GROUPS

Alternative expressions are permitted if they present no uncertainty or ambiguity with respect to the question of scope or clarity of the claims. One

EXHIBIT M

REDACTED

EXHIBIT N

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/080,774	05/18/98	BALAKIRSHNAN	B 233/248

EXAMINER

MM32/0818

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ART UNIT | PAPER NUMBER

2816 #6

DATE MAILED:

08/18/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/080,774	Balakrishnan et al.
Examiner	**Group Art Unit**
Jeffrey Zweizig	2816

☒ Responsive to communication(s) filed on 5/18/98 .

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 1 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-37 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☐ Claim(s) _____ is/are rejected.

☐ Claim(s) _____ is/are objected to.

☒ Claims 1-37 are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on 5/18/98 is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 3

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

U.S. Patent and Trademark Office
PTO-326 (Rev. 9-95) Office Action Summary Part of Paper No. 6

Drawings

1. Fig. 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Election/Restriction

2. This application contains claims directed to the following patentably distinct species of the claimed invention:

Group I: claims 1-10 & 29-37 directed toward a PWM circuit with a frequency variation circuit; and

Group II: claims 11-28 directed toward a PWM circuit with a soft start circuit.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claims are generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations

of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

3. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey Zweizig whose telephone number is (703) 305-7243. The examiner can normally be reached on Monday through Friday from 7:00 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

JZ

August 17, 1999

Jeffrey Zweizig

Patent Examiner

Art Unit 2816

MISSING PAGE(S) FROM THE

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#6 - PTO 948 FORM

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EXHIBIT O

#8

Attorney's Docket No. 003692.P036 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:
BALAKRISHNAN ET AL.
Application No.: 09/080,774
Filed: May 18, 1998
For: OFF-LINE CONVERTER WITH INTEGRATED SOFTSTART AND FREQUENCY JITTER

Examiner: Zweizig, Jeffrey.
Art Unit: 2816

Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT AND RESPONSE TO ELECTION REQUIREMENT

Drawing Objection

In response to the Election Requirement mailed August 18, 1999, it is proposed by the Examiner that Figure 1 be designated by a legend such as --Prior Art--. Accordingly, the Applicants submit a proposed drawing correction in the form of a red-mark original of Figure 1. The Applicants request the Examiner to approve the drawing. The Applicants will submit formal corrections for Figure 1, including any additional changes in response to form PTO-948, when the Application is allowed by the Examiner.

Restriction Requirement

In response to the Election Requirement mailed August 18, 1999, the Applicant hereby elects without traverse the invention of Group I, claims 1-10 and 29-37.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 11-2-99

James Y. Go
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231 on November 2, 1999

Melanie Beseckler 11-2-99
Melanie Beseckler Date

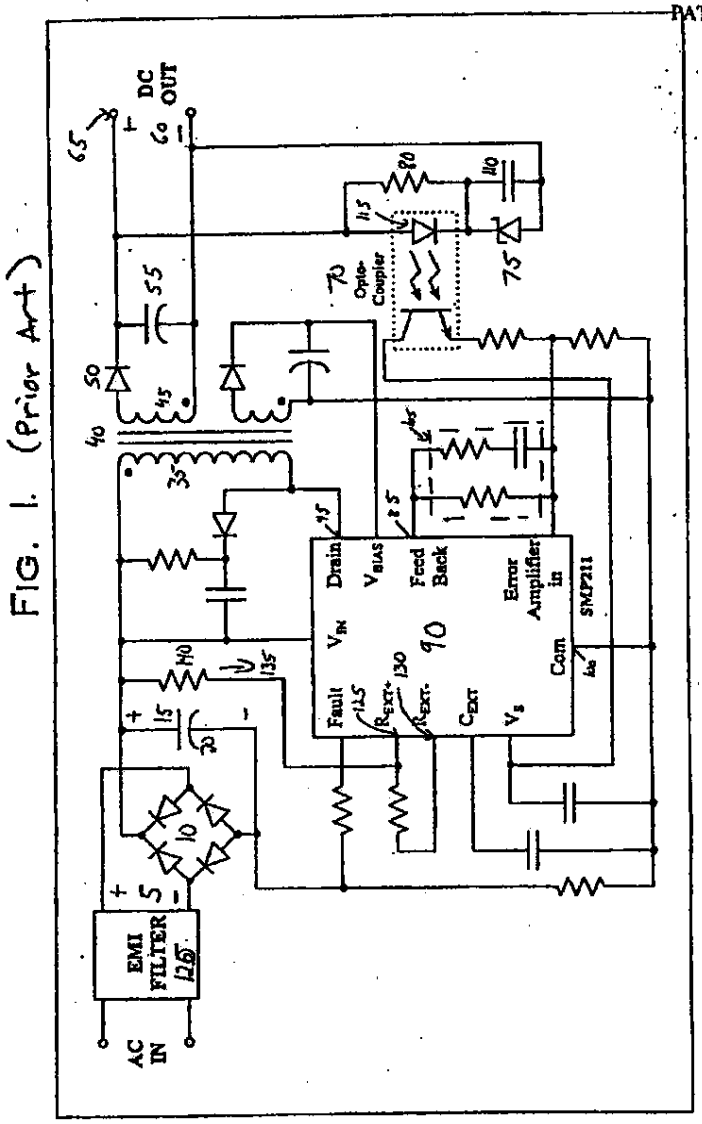

FIG. 1. (Prior Art)

EXHIBIT P

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
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Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/080,774	05/18/98	BALAKIRSHNAN	B 233/248

MM22/1213

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LOS ANGELES CA 90071

EXAMINER	
ZWEIZIG, J	
ART UNIT	PAPER NUMBER
2816	4

DATE MAILED: 12/13/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95) 1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/060,774	Balakrishnan et al.
Examiner	**Group Art Unit**
Jeffrey Zweizig	2816

☒ Responsive to communication(s) filed on *11/8/99*.

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-37* is/are pending in the application.

Of the above, claim(s) *11-28* is/are withdrawn from consideration.

☒ Claim(s) *1-3, 7, 8 & 10* is/are allowed.

☒ Claim(s) *4-6, 9 & 29-37* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☒ The proposed drawing correction, filed on *11/8/99* is ☒approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

U. S. Patent and Trademark Office
PTO-326 (Rev. 9-95) Office Action Summary Part of Paper No. 9

Election/Restriction

1. This application contains claims directed to the following patentably distinct species of the claimed invention:

Group I: claims 1-10 & 29-37 directed toward a PWM circuit with a frequency variation circuit; and

Group II: claims 11-28 directed toward a PWM circuit with a soft start circuit.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claims are generic. Applicants have elected, without traverse, Group I: claims 1-10 & 29-37. Claims 11-28 have been withdrawn from consideration.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4-6, 9 & 29-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4 lines 2 & 3, "a magnitude of said oscillation signal" should be changed to --said magnitude of said oscillation signal--.

In claim 9 line 8, "pulse width modulated switch" should be changed to just --switch-- (see claim 1 line 4).

In claim 9 line 9, the second occurrence of "first winding" should be changed to --second winding--.

Refferring to the phrase "said first [second] winding capable of being coupled to a load", it is not understood if the winding is or is not coupled to the load.

In claim 29, the phrase "that provides a drive signal for a maximum time period of a time duration signal" is not understood. If the drive signal were applied for the maximun period of the duration, the drive signal would always be applied.

In claim 35 line 8, "regulation circuit" should be changed to just --switch-- (see claim 29 line 4).

In claim 35 line 9, the second occurrence of "first winding" should be --second winding--.

Refferring to the phrase "said first [second] winding capable of being coupled to a load", it is not understood if the winding is or is not coupled to a load.

Claims 4, 9, 29 & 35 are indefinite. Claims 5, 6 & 30-37 are rejected as being dependent on an indefinite intervening claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 29, 35 & 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicants' Prior Art Fig. 1.

Applicants' Prior Art Fig. 1 shows a first terminal 95, a second terminal Com, a switch/drive circuit 90 and a frequency variation circuit 140 as recited in claim 29.

Further shown is a rectifier 10, a capacitor 15, a first winding 35 and a second winding 45 as recited in claim 35.

Further shown is a feedback terminal (Error Amplifier in) as recited in claim 37.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Prior Art Fig. 1.

Applicants' Prior Art Fig. 1 does not specify that the circuit is an integrated circuit as recited in claim 34. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Prior Art Fig. 1 as an integrated circuit for the benifit of implementing a compact single package. Claim 34 is obvious.

Allowable Subject Matter

8. The prior Art of record does not appear to disclose or suggest a PWM switch comprising an oscilator for generating a maximum duty cycle signal and a singnal with a frequency range dependent on a frequency variation circuit as recited in claim 1.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey Zweizig whose telephone number is (703) 305-7243. The examiner can normally be reached on Monday through Friday from 7:00 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

JZ

December 13, 1999

Jeffrey Zweizig

Patent Examiner

Art Unit 2816

Notice of References Cited

Application No. 09/080,774	Applicant(s) Balakrishnan et al.	
Examiner Jeffrey Zweizig	Group Art Unit 2816	Page 1 of 1

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
	A	---	---	None	---	---
	B					
	C					
	D					
	E					
	F					
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PTO-892 (Rev. 9-95) Notice of References Cited Part of Paper No. 9

EXHIBIT Q

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